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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/466,234	12/17/1999	MARK A. BEILEY	42390.P8081	9912

7590 05/18/2005

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EXAMINER	
STULBERGER, CAS P	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/466,234	BEILEY ET AL.	
	Examiner	Art Unit	
	Cas Stulberger	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,9,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,9,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: application, filed 12/17/1999; Request for Consideration filed 04/08/2005.

2. Claims 1, 4-6, 9, 12-13 are pending in the case. Claims 2-3, 7-8, 10-11, and 14-15 have been cancelled. Claims 1, 5, 9, and 12 are independent claims.

Response to Amendment

3. Applicant also argues that Piosenka does not disclose or suggest "wherein the reference voltage is a voltage at a node of a second capacitor." Applicant's arguments, see Request for Continued Examination, filed 04/08/2005, with respect to the rejection(s)of claim(s) 1, 4-6, 9, 12, and 13 under 35 U.S.C 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-6, 9, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,389,738 to Piosenka et al in view of U.S. Patent No 4,353,056 to Tsikos.

6. In regards to claims 1, 4-6, 9, 12, and 13 Piosenka disclosed a tamperproof arrangement for an integrated circuit device (Piosenka: Abstract). A dielectric layer is placed between two grid layers as shown in Figure 2. This meets the limitation of "a first capacitor formed with a dielectric including the dielectric encasing elements of the circuit; approximately parallel conductors located proximate to circuit elements to protect from tampering." Attempts to penetrate this grid electrode finger structure will break the conductive path or remove a significant portion of a conductor and/or change the capacity or resistance between the top and bottom grids. Detectors will detect changes in the capacitance or resistance and trigger zeroizing or clearing of all sensitive or confidential information within the integrated circuit thereby rendering the integrated circuit of no use to an attacker (Piosenka: column 3, lines 12-45). This meets the limitation of "a detector to detect changes in the capacitance of the capacitor." Piosenka discloses that comparators are located within the critical circuit function area (Piosenka: column 6, lines 7-8). The comparators constantly monitor the voltage output of sensors and compare this output to the reference voltage of the zener diode (Piosenka: column 4, lines 63-66). This meets the limitation of "a comparator to compare a reference voltage with a voltage at a node of the first capacitor." However Piosenka does not disclose "wherein the reference voltage is a voltage at a node of a second capacitor."

Tsikos however discloses an array of capacitors. The capacitors are all charge to the same capacitance and voltage (reference voltage) (Tsikos: column 3, lines 22-31). A multiplexor determines a change in the capacitances when the distance between them is changed and therefore the Voltage of the capacitors changes as well (Tsikos: column 28-35). This meets the limitation of "wherein the reference voltage is a voltage at the node of a second capacitor."

7. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the method of comparators monitoring the voltage output of sensors and comparing them to the reference voltage as disclosed by Piosenka with the method of using capacitors to hold the reference voltage as disclosed by Tsikos because such sensors are easy to manufacture (Tsikos: column 4, lines 45-46).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cas Stulberger whose telephone number is (571) 272-3810. The examiner can normally be reached on Monday - Friday, 9:00A.M. - 6:00P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3810. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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